The evaluation board for TOSHIBA　TMPM369FDFG user's manuals

Revision 1.2.0

2014/11/27

A product specification is an object of change without a preliminary announcement

・Introduction

This manual is a user's manual of the evaluation board for Toshiba TMPM369FDFG.

・Table of contents

・Revision history

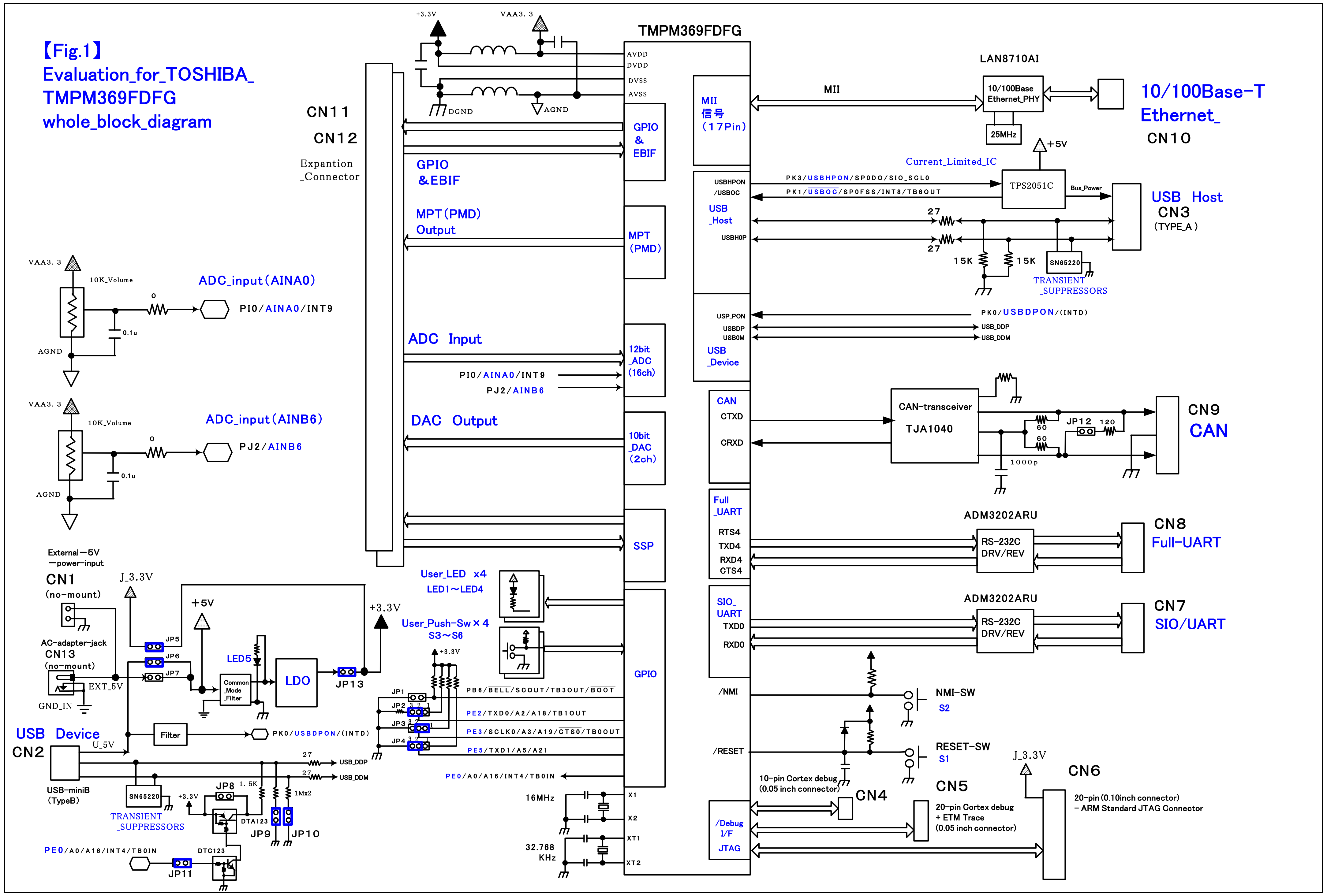
Date	Revision	Sheet numbe	Contents
2012/9/12	Revision 1．00		First edition creation
2013/4/25	Revision 1．10		default jumper configuration JP5:OPEN →JP5:CLOSE
2014/11/27	Revision 1．20	p7 p9	5, 16-bit timer (TMRB) 16 channels -> 8 channels 24, Interruption function ・ 110 kinds of insides -> 112 kinds of insides ・ 17 kinds of exteriors : (NMI is included). -> 16 kinds of exteriors : (NMI is excluded) 33, Package ・LQFP144-P-2020-0.5 -> LQFP144

Chapter 1, Outline

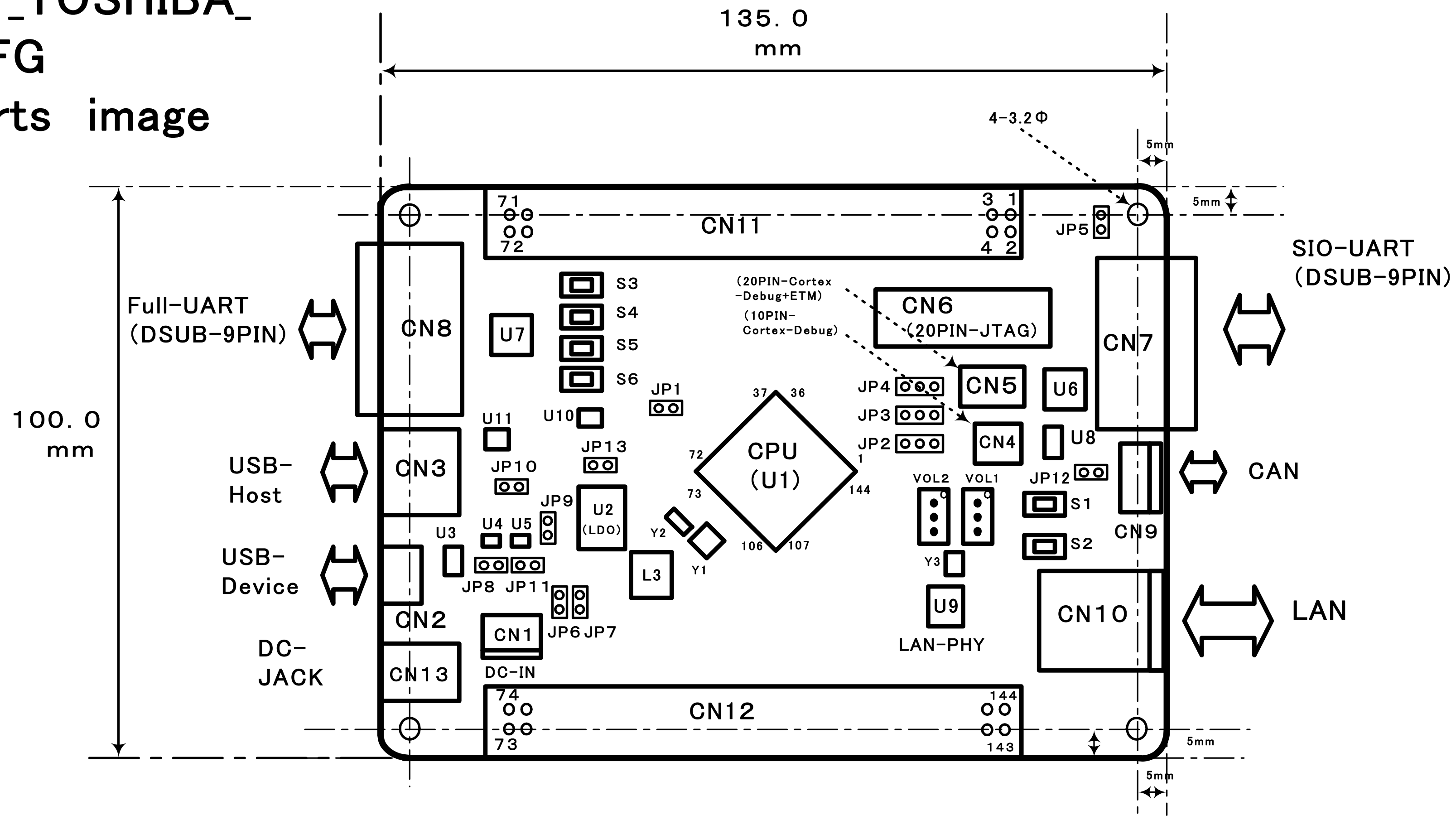
Evaluation Board for TOSHIBA TMPM369FDFG enable you to create and test working programs based on the Toshiba TMPM360 family of ARM Cortex™-M3 processor-based devices

【Features】

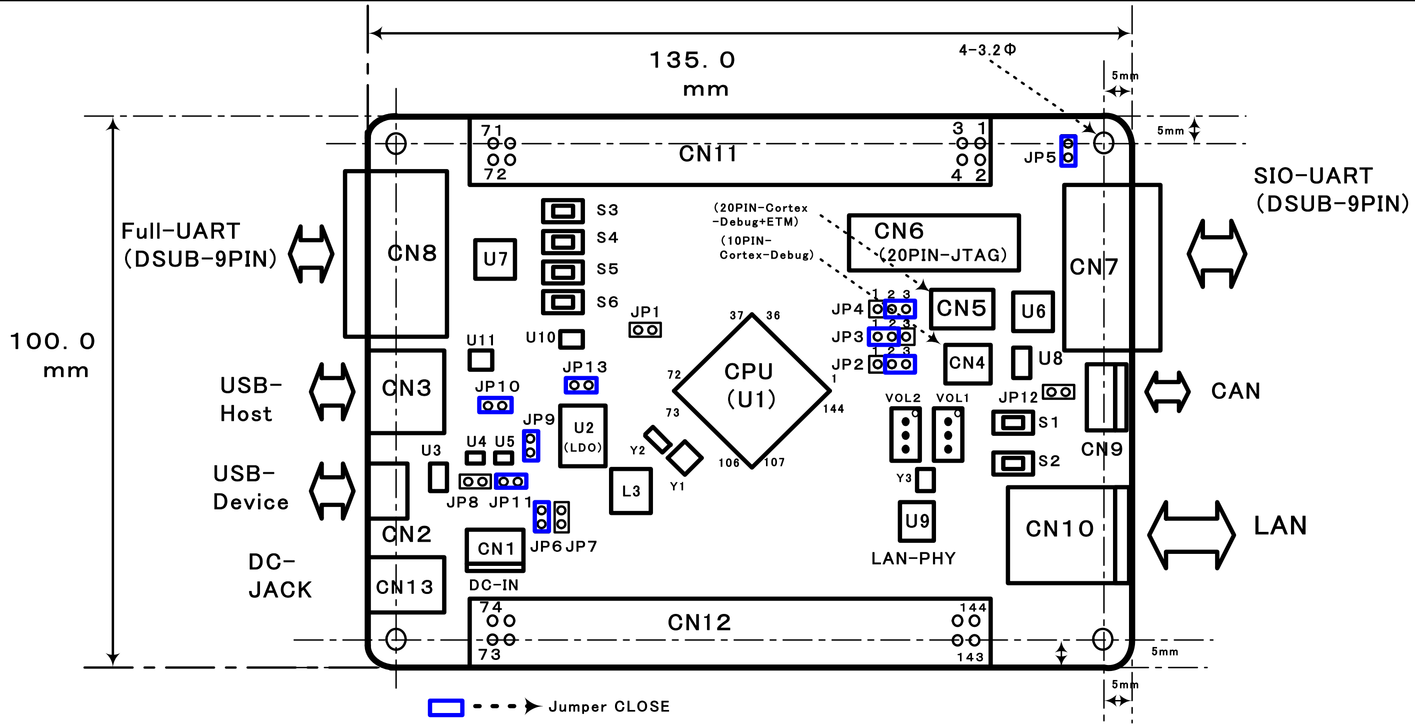
- 80MHz ARM Cortex™-M3 processor-based MCU in 144-pin LQFP
- On-Chip Flash: 512KB (TMPM369FDFG)
  On-Chip Flash: 256KB (TMPM369FYFG)
- On-Chip RAM: 128KB (TMPM369FDFG)
  On-Chip RAM: 64KB (TMPM369FYFG)
- USB 2.0 Host
- USB 2.0 Device
- CAN 2.0B Interface
- EterMAC (10/100Base-T)
  On a board LAN-PHY made from SMSC (LAN8710A) is mounted.
- 12bit ADC(16ch : AINA0〜AINA3, AINB0〜AINB11)
  Multi-rotation volume for ADC Input(2ch-only:AINAO、AINB6)
- 10bit DAC(2ch : DAO, DA1)
- SIO/UART ch0〜ch3
  Only the channel 0 equips DSUB-9pin connector with a RS-232C driver / receiver..
- Full/UART ch4〜ch5
  Only the channel 4 equips DSUB-9pin connector with a RS-232C driver / receiver..
- 5 LEDs and 6 push-buttons
  LED1〜LED4 --- Status display LED (This LED is connected to PC7〜PC4 of a port.)
  LED5 :LED for power light
  S1: Push switch for /reset
  S2: Push switch for /NMI
  S3〜S6 : Push switch for a test
- Power via USB connector
  As an option An AC adaptor jack (CN13)
  and an external 5V-Power input connector (CN1) are equipped.
  (However, in order to usually perform electric supply from a USB connector,
  CN1 and CN13 suppose un-mounting.)
- Debug Interface Connectors
  - 10-pin Cortex debug (0.05 inch connector)
  - 20-pin Cortex debug + ETM Trace (0.05 inch connector)
  - 20-pin (0.10inch connector) - ARM Standard JTAG Connector


【Fig.1】
Evaluation_for_TOSHIBA_
TMPM369FDFG
whole_block_diagram
TMPM369FDFG
CN11
CN12
Expantion
_Connector
GPIO
&EBIF
MPT(PMD)
Output
ADC Input
DAC Output
LAN8710AI
10/100Base-T
Ethernet_
CN10
MII
USB Host
CN3
(TYPE_A)
Current_Limited_IC
TPS2051C
TRANSIENT
_SUPPRESSORS
ADC_input(AINA0)
PI0/AINA0/INT9
ADC_input(AINB6)
PJ2/AINB6
CAN-transceiver
TJA1040
CN9
CAN
ADM3202ARU
RS-232C
DRV/REV
CN8
Full-UART
CN7
SIO/UART
User_LED x4
LED1~LED4
User_Push-Sw×4
S3~S6
External-5V
-power-input
CN1
(no-mount)
AC-adapter-jack
CN13
(no-mount)
LDO
JP13
USB Device
CN2
USB-miniB
(TypeB)
NMI-SW
S2
RESET-SW
S1
CN4
10-pin Cortex debug
(0.05 inch connector)
CN5
20-pin Cortex debug
+ ETM Trace
(0.05 inch connector)
CN6
20-pin (0.10inch connector)
- ARM Standard JTAG Connector
16MHz
32.768
KHz

【Fig. 2】
Evaluation_for_TOSHIBA_
TMPM369FDFG
PCB Main parts image



U1	CPU	TMPM369FDFG (TMPM369FYFG)	TOSHIBA
U2	LDO	LD1117S33CTR	ST-Microelectronics
U3	USB-Transient-Suppressor	SN65220DBVT	TI
U4	Digital Transistor PNP	DTA123EE	Rohm
U5	Digital Transistor NPN	DTC123EE	Rohm
U6	RS-232C Line Drivers/Receivers	ADM3202ARUZ	Analog Devices Inc
U7	RS-232C Line Drivers/Receivers	ADM3202ARUZ	Analog Devices Inc
U8	CAN TRANSCEIVER	TJA1040T	NXP Semiconductors
U9	LAN-PHY	LAN8710AI	SMSC
U10	Current-Limited, Power-Distribution-Switches	TPS2051CDBVT	TI
U11	USB-Transient-Suppressor	SN65220DBVT	TI



【Fig. 3】
Evaluation_for_TOSHIBA_
TMPM369FDFG
Jumper configration (default)

Default configuration
JP1:OPEN → Normal
JP2 :2−3 CLOSE → X1 OSC select
JP3:1−2 CLOSE → X1 OSC(16＊3)
JP4:2−3 CLOSE → SIO BOOT
JP5:CLOSE → Target_board power supply to CN6-1PIN
JP6:CLOSE → It supplies from a USB Device connector (CN2)

JP7:OPEN → With no electric supply
JP8:OPEN → With no pull-up
JP9:CLOSE → USB_DP terminal 1MΩ pull-down
JP10:CLOSE → USB_DM terminal 1MΩ pull-down
JP11:CLOSE → Control port (PE0) It is used.
JP12:OPEN → Termination is not used.
JP13:CLOSE → The regulator output on a board is used

【Table. 1】

Evaluation Boardfor TOSHIBA TMPM369FDFG

【 Jumper pin setting table】

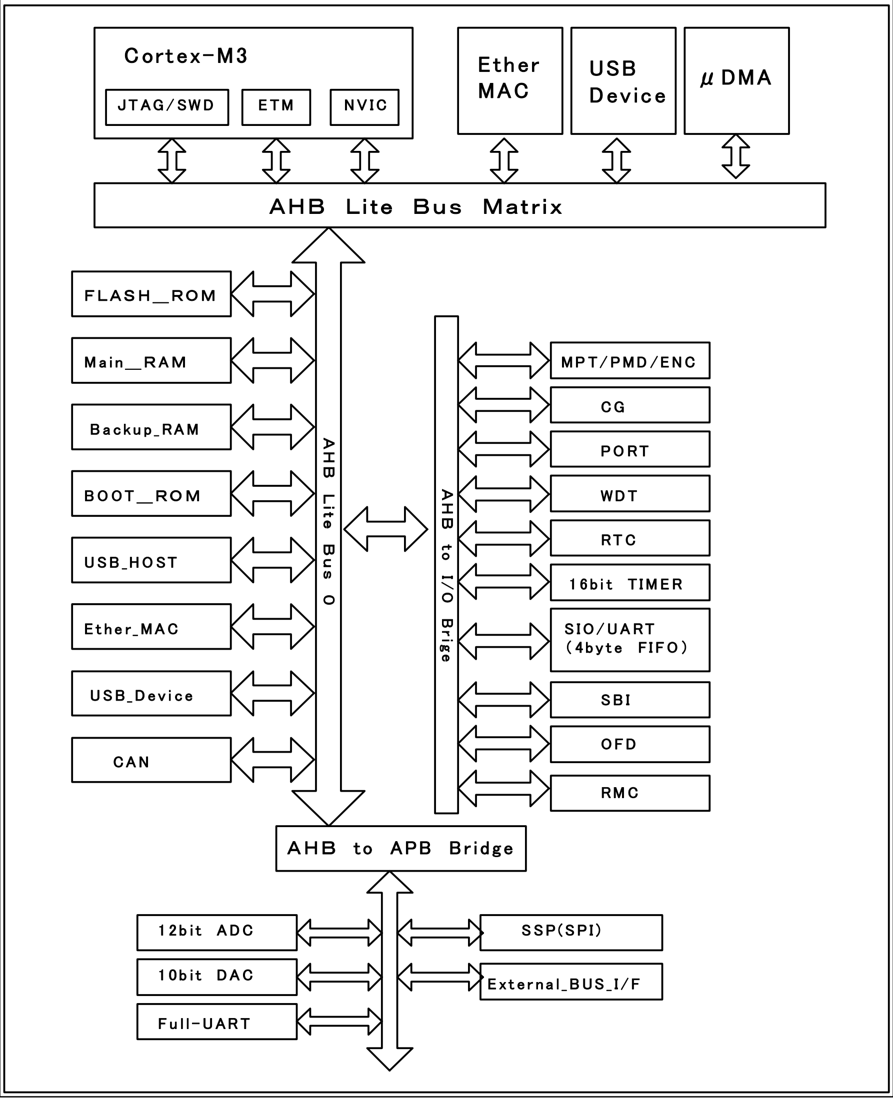
	Reference	The number of pins	Silk name	Function
	JP1	2PIN	JP1 /BOOT	･Boot mode select JP1:OPEN → Normal JP1:CLOSE → BOOT Mode
	JP2	3PIN	JP2 1 USBCLK 2 3 X1 OSC	･Selection of a clock JP2:1−2 CLOSE→ USBCLKI JP2:2−3 CLOSE→ X1 OSC
	JP3	3PIN	JP3 1 X1 OSC(16＊3) 2 3 USB_ECLK	･USB Clock selection JP3:1−2 CLOSE→ X1 OSC(16＊3) JP3:2−3 CLOSE→ USB_ECLK
	JP4	3PIN	JP4 1 USB_BOOT 2 3 SIO_BOOT	･Boot mode kind selection JP4:1−2 CLOSE→ USB BOOT JP4:2−3 CLOSE→ SIO BOOT
	JP5	2PIN	JP5 JTAG_POWER	･3.3V target supply source selection JP5:OPEN → With no target supply to CN6-1pin JP5:CLOSE → It supplies target +3.3V-power to JTAG(CN6-1pin)
	JP6	2PIN	JP6 USB_5V	･5V electric supply source selection JP6:OPEN → With no electric supply JP6:CLOSE → It supplies from a USB Device connector (CN2)
	JP7	2PIN	JP7 EXT_5V	･5V electric supply source selection JP7:OPEN → With no electric supply JP7:CLOSE → It supplies 5V from an external connector (CN1 or CN13).
	JP8	2PIN	JP8 DP_PULL-UP	･USB_DP terminal 1．5KΩ Compulsive pull-up JP8:OPEN → With no pull-up JP8:CLOSE → USB_DP terminal Compulsive pull-up
	JP9	2PIN	JP9 DP_PULL-DOWN	･USB_DP terminal 1MΩPulldown JP9:OPEN → With no pull-down JP9:CLOSE → USB_DP terminal 1MΩ pull-down
	JP10	2PIN	JP10 DM_PULL-DOWN	･USB_DM terminal 1MΩPulldown JP10:OPEN → PULL-DOWN無し JP10:CLOSE → USB_DM terminal 1MΩ pull-down
	JP11	2PIN	JP11 PE0−EN	･USB_DP terminal Compulsive pull-up control port (PE0) enabling JP11:OPEN → Control port (PE0) It is not used. JP11:CLOSE → Control port (PE0) It is used.

Chapter 2, Hardwar discription

The TMPM369FDFG is a 32-bit RISC microprocessor series with an ARM Cortex-M3 microprocessor core. .

The internal composition of CPU is shown in Fig.4.

【Fig. 4】 TMPM369FDFG CPU internal block_diagram



【CPU functional outline】

1, ARM Cortex-M3 microprocessor core

(a), . Improved code efficiency has been realized through the use of Thumb-2 instruction.

- New 16-bit Thumb instructions for improved program flow
- New 32-bit Thumb instructions for improved performance
- New Thumb mixed 16- / 32-bit instruction set can produce faster, more efficient code.

(b), . Both high performance and low power consumption have been achieved.

[High performance]

- Both high performance and low power consumption have been achieved.
- Division takes between 2 and 12 cycles depending on dividend and devisor

[Low Power consumption]

- Optimized design using a low power consumption library
- Standby function that stops the operation of the micro controller core

(c), ..High-speed interrupt response suitable for real-time control

- An interruptible long instruction
- Stack push automatically handled by hardware

2, **High-speed writing which demonstrates an effect at the time of high-speed write-in & low power consumption and mass production by Toshiba NANO FLASH- technology, and development**

3, On Chip program memory and data memory

- On-Chip Flash: 512KB (TMPM369FDFG)
  On-Chip Flash: 256KB (TMPM369FYFG)
- On-Chip RAM: 128KB (TMPM369FDFG)
  On-Chip RAM: 64KB (TMPM369FYFG)

4, DMA controller (DMAC): 32 channel / 2 unit

The candidate for transmission: A built-in memory, built-in I/O, and an external memory

5, 16-bit timer (TMRB) : 8 channels

- 16-bit interval timer mode
- 16-bit event counter mode
- 16-bit PPG output (4channel timer can start synchronously)
- Input capture function

6, Real time clock (RTC) : 1channel

- Clock (hour, minute and second)
- Calendar (month, week, date and leap year)
- Alarm (Alarm output)
- Alarm interrupt

7, Watchdog timer (WDT) : 1 channel

Watchdog timer (WDT) generates a reset or a non-maskable interrupt (NMI).

- 26 Stage binary counter
- Watchdog timer out function

8, **General-purpose serial interface (SIO/UART) : 4 channels**

Either UART mode or synchronous mode can be selected (4byte FIFO equipped)

9, Serial bus interface (I2C/SIO):: 3 channels
Either I2C bus mode or synchronous mode can be selected.

10, Synchronous serial port (SSP) : 3 channels
Support SPI / SSI / Microwire

11, Full UART:2 Channel
8－Line Type UART / IrDA 1.0 Mode Select is Possible.

12, 10-bit AD converter (ADC) : 16 channels
・Start by an internal timer trigger
・Fixed channel / scan mode
・Single / repeat mode
・AD monitoring 2 channels
・Conversion speed 1.0 μsec (@ fsys = 80 MHz、Normal_Mode)
･Fast conversion by interleave mode (conversion time : a maximum of 0.5microsec)

13, 10bit DA Converter (DAC) : 2 Unit (2 Channel)
・ VREFH cut function (Power down mode)
・ Output current : 1 mA
・ Seduced time : 1microsec
・ Signal generation function

14, USB2.0 Full Speed Device : 1 Channel
・ It is based on Universal Serial Bus Specification Rev2.0.
・ End point : 8 channel
・ Control/Bulk/Interrupt/Isochronus mode
・ Full speed 12Mbps (low speed is un-supporting)

15, USB host controller : 1 channel
・Universal serial bus (Rev 2.0 standard)
・Open HCI for USB Release 1.0a
・･Control/Bulk/Interrupt/Isochronus mode
・12Mbps(full speed) :(Low speed is un-supporting)

16, CAN : 1 channel
・Version 2.0B supported
・32 mail boxes
・Maximum transfer speed : 1 Mbps

17, Ethernet MAC:1 Channel
・ IEEE802.3u conformity
・ Flow control (IEEE802.3x / back pressure system)
・ 10Mbps / 100Mbps correspondence
・ MII (Media Independent Interface) correspondence
・ High-speed communication by exclusive DMA and a total of 8-K byte FIFO
・ Magic packet detection function

18, Remote Control Judging Function (RMC) : 1 Channel
・ It is package reception to ７2bit.
・ Noise canceller function
・ Reader code detection function

19, Multiple-purpose - timer (MPT):4 channel
・motor control (PMD:2 channel)
・IGBT control
・16-bit timer

20, Encoder input function: 2 channel
・Incremental form encoder correspondence

21, LVD/POR Function : 1 Unit

22, Oscillation Frequency Detection : 1 Unit

23, External bus interface: : 1 unit
・separation / multiplexer bus : 8 bit / 16 bit width
・ chip select / wait controller: : 4 channel

24, Interruption function
・ 112 kinds of insides : a priority setup of 7 level is possible.
(Watchdog timer interruption is excluded)
・ 16 kinds of exteriors : a priority setup of 7 level is possible (NMI is excluded)

25, Input / output ports (PORT)
・I/O port : 101 pins
・Output port : 1 pins

26, Standby function
・Standby mode : IDLE, STOP1, STOP2
・IDLE ::CPU stop
・STOP1/STOP2:: All the circuit stops except RTC and a remote control judging circuit
(STOP2 At the time of the mode in part a circuit power supply interception)

27, Clock Generator
・ PLL built-in (3, 4, 5, 6, 8, and 10times PLL frequency change is possible)
・ Clock gear function : dividing is possible in a high-speed clock to 1/1, 1/2, 1/4, 1/8, and 1/16.

28, Endian
・Little endian

29, Debugging interface
・JTAG/SWD/SWV/TRACE(DATA 4bit)

30, Maximum operating frequency
・80 MHz
(the time of external oscillator 8MHz, 10 MHz, or 16MHz use
or built-in oscillator 10MHz use)

31, The range of operating voltage
・2.7V～3.6V (at the time of USB functional disuse)
・3.0V～3.6V (at the time of USB functional use)

32, Operating temperature range
・ −40℃～˜ 85℃ (Except the time of flash writing / erase)
・ 0℃ ～ 70℃ (At the time of flash writing / erase)

33, Package
・LQFP144 (20mm x 20mm, 0.5mm pitch)